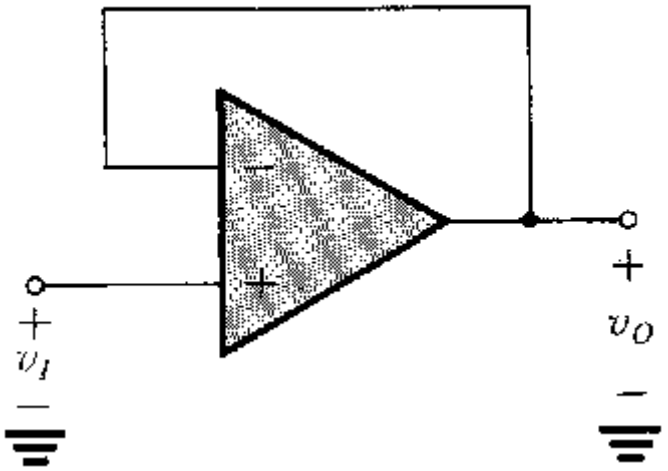
Slew Rate

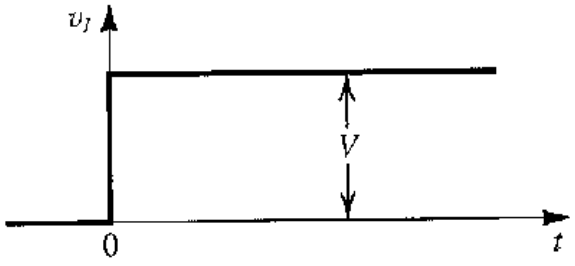


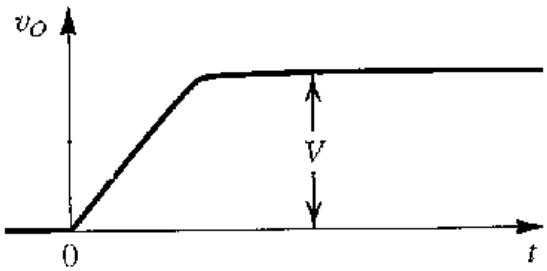
$$\frac{v_O}{v_I} = \frac{1}{1+\frac{s}{\omega_t}} \qquad (1)$$

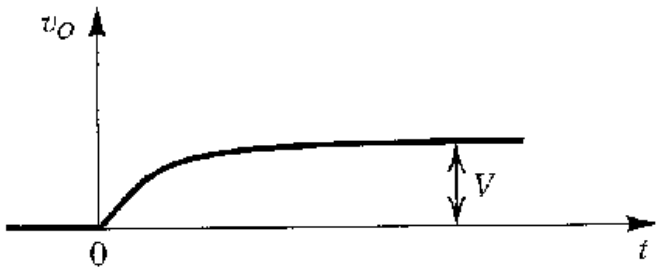
if $v_I(t) = V \cdot u(t)$ (2)

then $v_O(t) = V(1-e^{-t/\tau})$ (3)

where $\tau = 1/\omega_t$



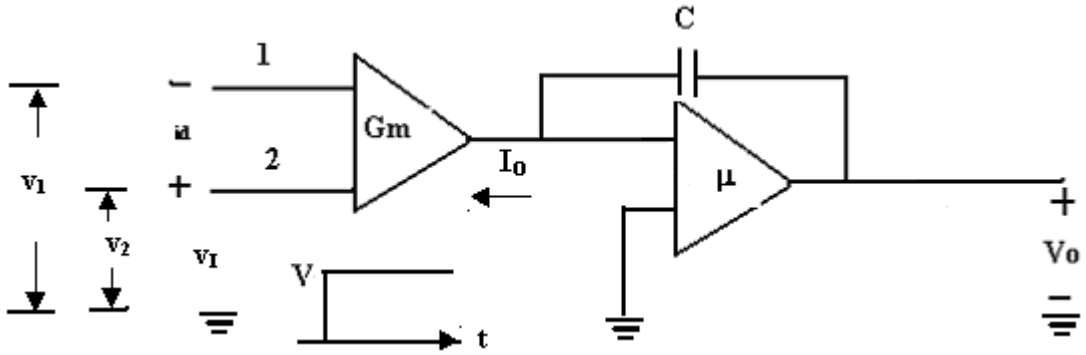




For V large, the op amp output will be unable to rise at the rate predicted by equation 3. When the op amp output is unable to rise at the rate predicted by equation 3, i.e., V/τ (ω_t=0), it is said to be slew-rate limited – or slewing.

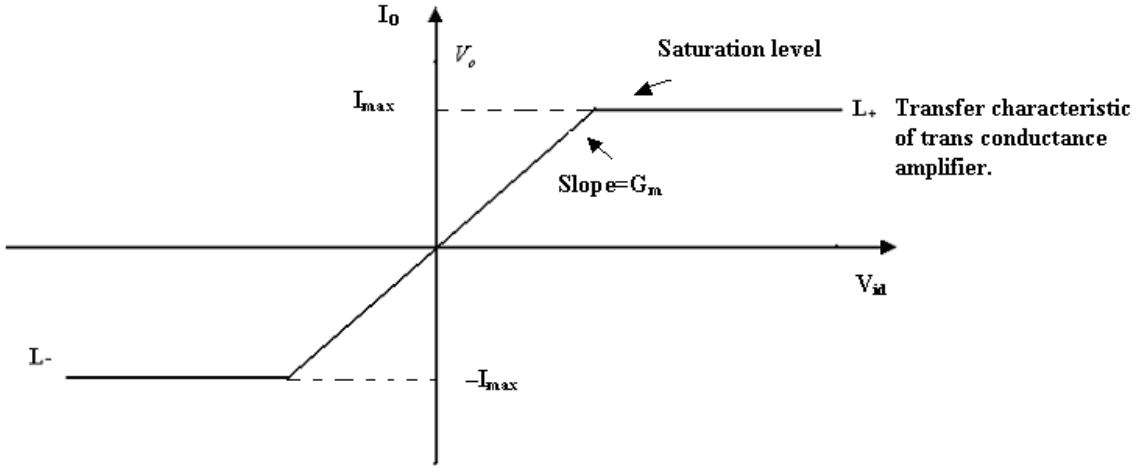
The slew-rate (SR) is the maximum possible rate of change of the op amp output voltage.

$$SR = \left.\frac{dv_O}{dt}\right|_{\max} \qquad V/\mu\text{sec}$$



Origin of slew rate

At t = 0, $v_2=v_I=V$, $v_O=0$; i.e., $v_1=0$, $\therefore v_{id}=V$
$\therefore$ the trans conductance will saturate.



$\therefore I_O = I_{max}$

$$v_O(t) = \frac{1}{C}\int i dt$$

Hence

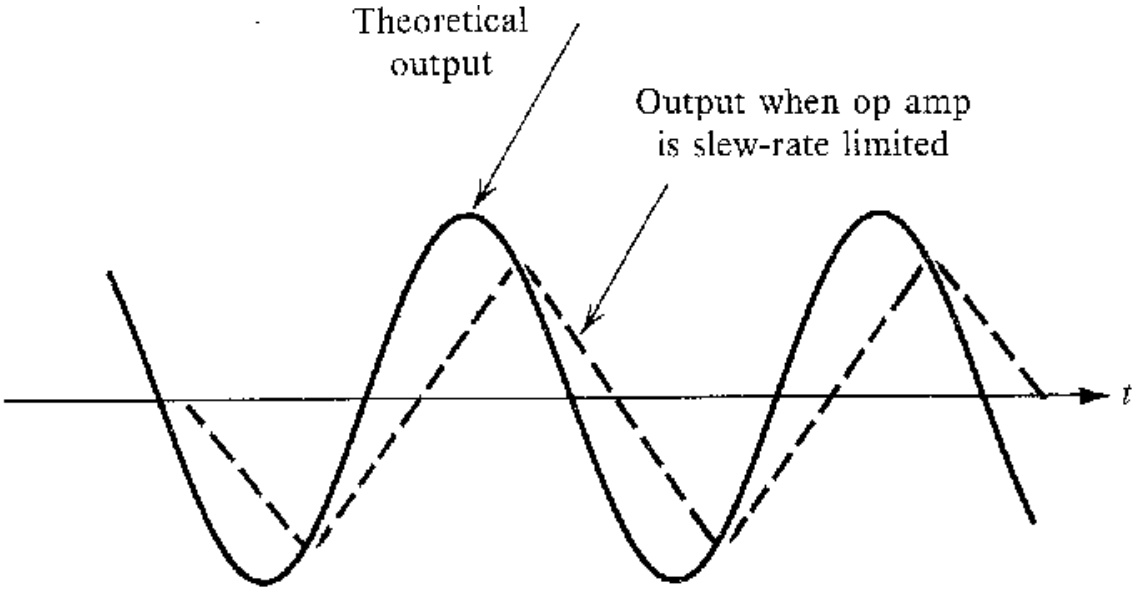
$$= \frac{1}{C}\int_0^t I_{\max} \cdot dt = \frac{I_{\max}}{C} \cdot t \qquad or \quad SR = \frac{I_{\max}}{C}$$

Full-Power Bandwidth

Op-amp slew-rate limiting can cause nonlinear distortion in sinusoidal waveforms.

$$v_I = \hat{V}_i \sin \omega t$$

$$\frac{dv_I}{dt} = \omega \hat{V}_i \cos \omega t$$



$$\left.\frac{dv_I}{dt}\right|_{\max} = \omega \hat{V}_i$$

$$also \quad \left.\frac{dv_O}{dt}\right|_{\max} = \omega \hat{V}_o$$

The frequency at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting is called the full-power bandwidth, f_M.

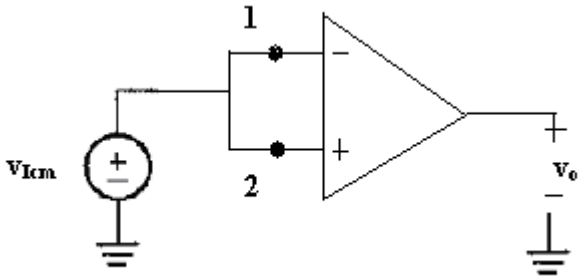
$$\omega_M V_{o\max} = SR$$

$$\therefore f_M = \frac{SR}{2\pi V_{o\max}}$$

For $V_o < V_{omax}$ (= rated o/p voltage), slew rate distortion will appear at a frequency ω given by:

$$\omega V_o = SR$$
$$\text{or } \omega V_o = \omega_M V_{omax}$$
$$\text{i.e., } V_o = V_{omax}(\omega_M/\omega)$$

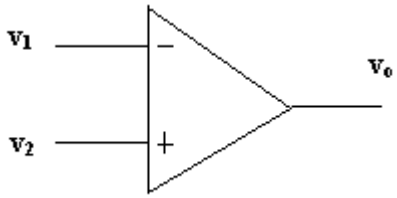
COMMON-MODE REJECTION



A_{cm} = common-mode gain = v_o/v_{Icm}

vid = v_2-v_1

$v_{Icm} = (v_2+v_1)/2$

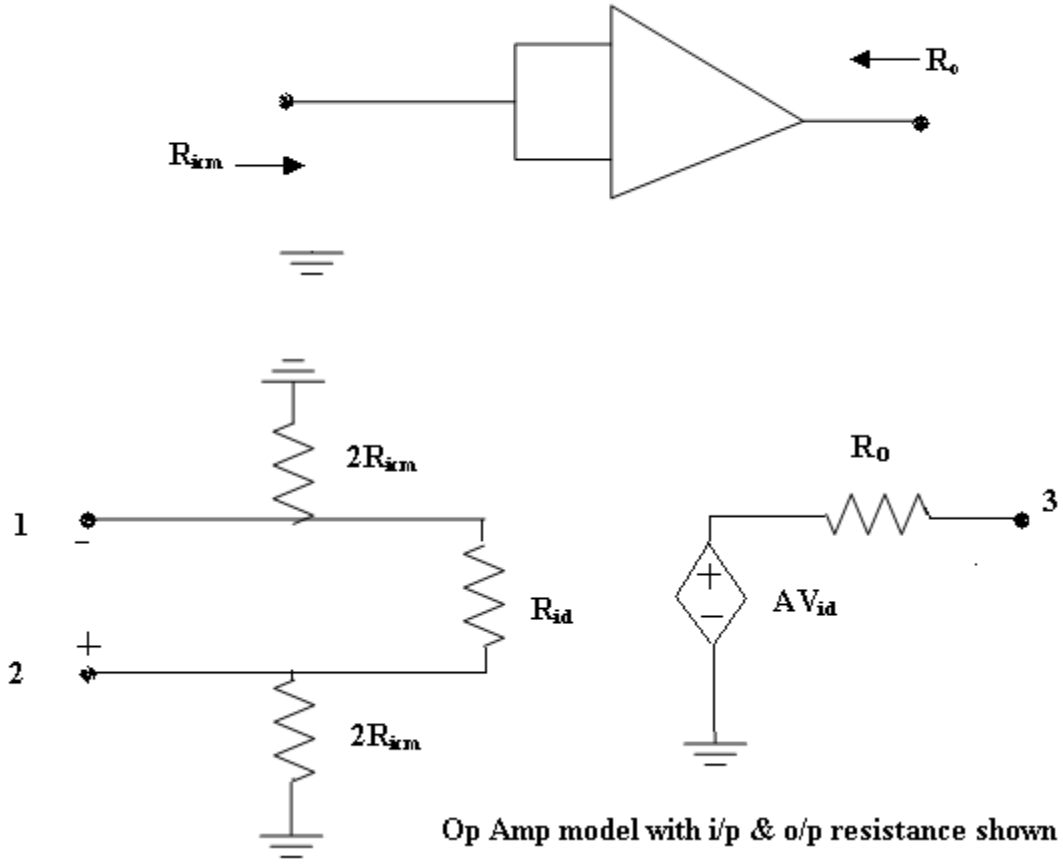


$v_o = Av_{id} + A_{cm}v_{Icm}$

Common-mode rejection ratio (CMRR)

$$CMRR = \frac{|A|}{|A_{cm}|} \quad \text{or in dB, } = 20\log_{10}\frac{|A|}{A_{cm}}$$

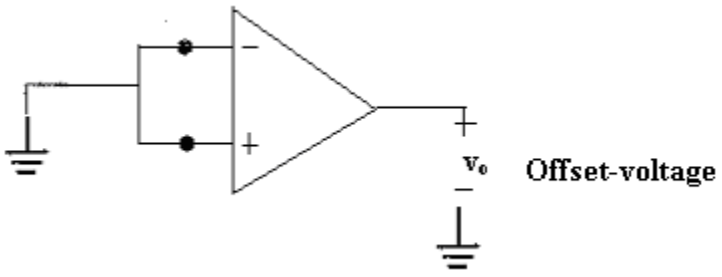
INPUT AND OUTPUT RESISTANCES

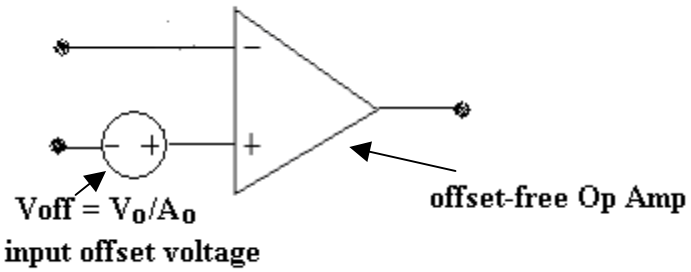


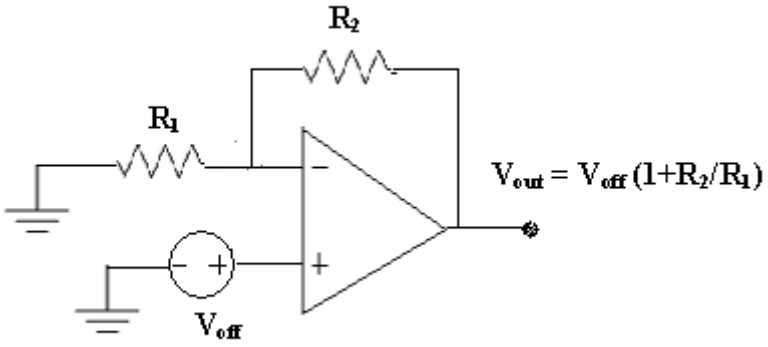
Op Amp model with i/p & o/p resistance shown

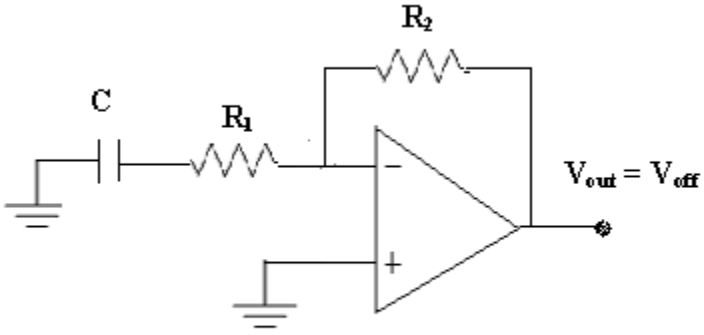
DC Problems

Offset voltage:



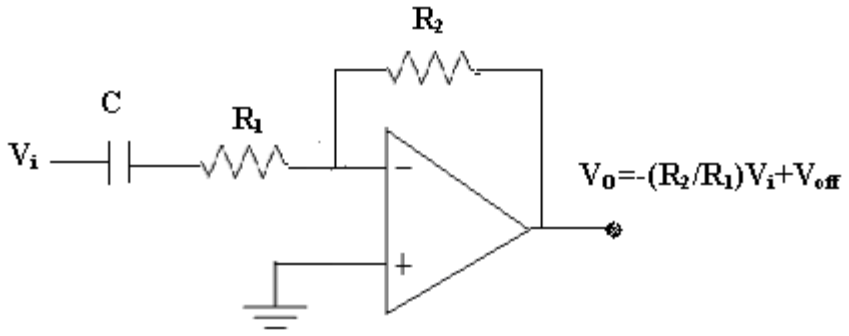






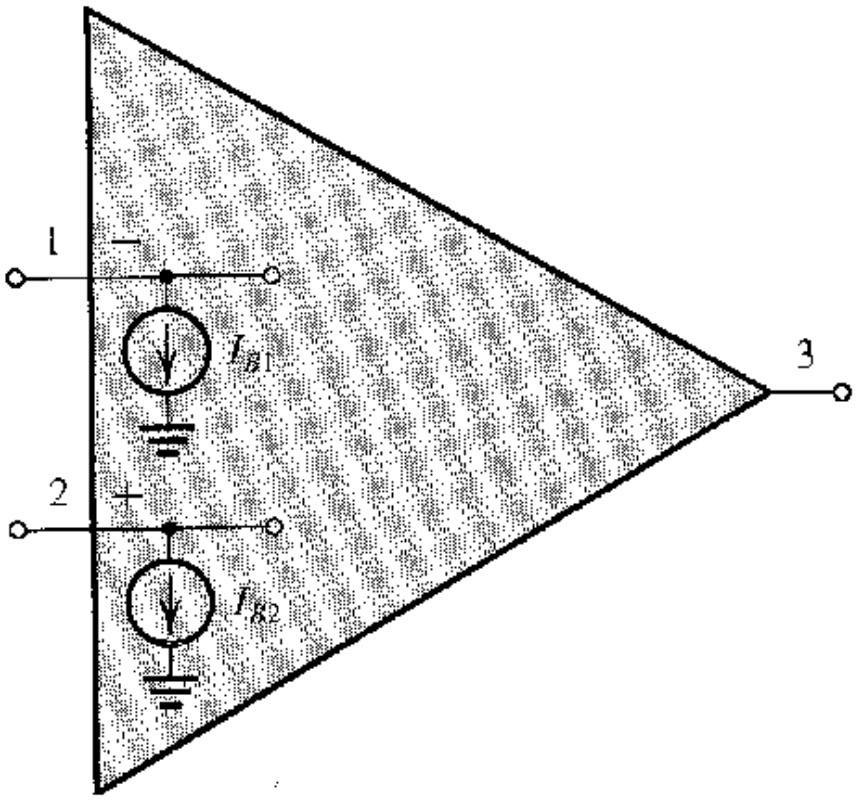
In this arrangement, V_{off} will be amplified.

The DC output offset will change the bias conditions and drive the amplifier to saturation. To avoid this problem, we capacitively coupled amplifiers.



C is selected large enough to appear almost as a short circuit for input frequencies – i.e., $\frac{1}{\omega C} \approx 0 \qquad \omega \in [\omega_{\min}, \omega_{\max}]$.

Input Bias Currents

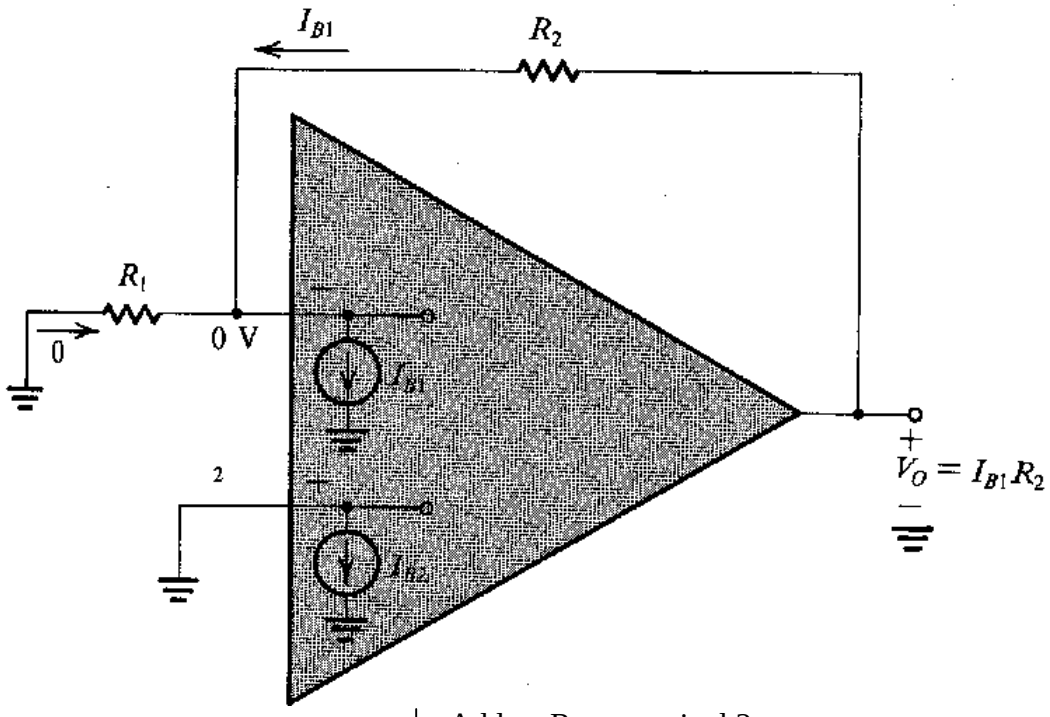


The average value I_B is called the input bias current. $I_B = \frac{I_{B1} + I_{B2}}{2}$

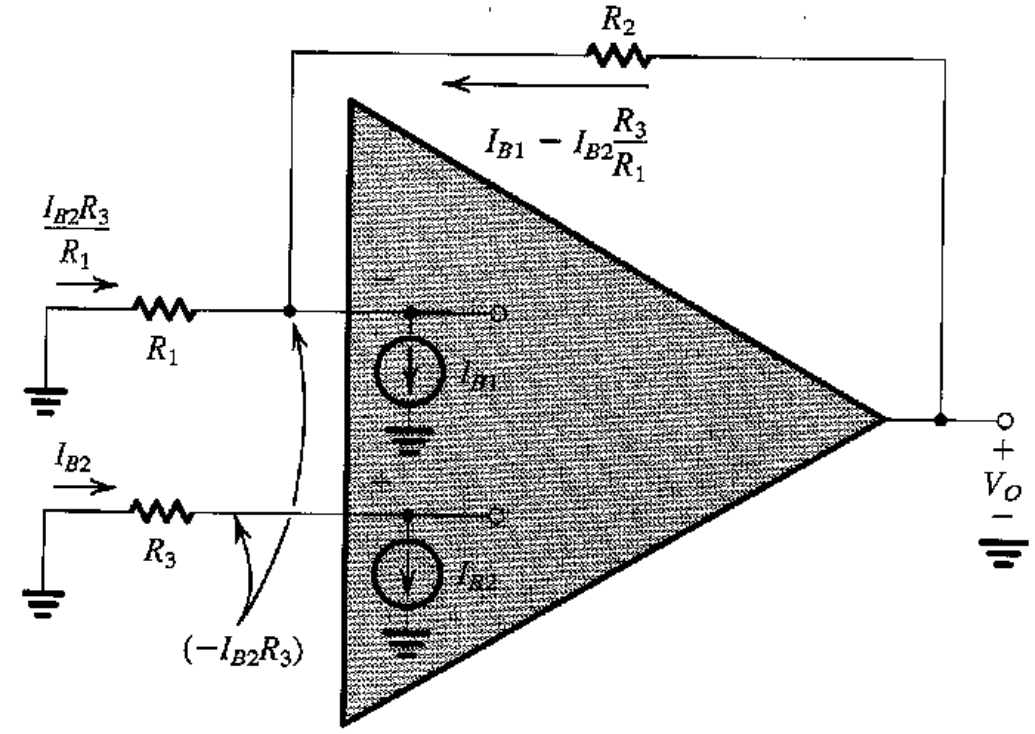
Input offset current: $I_{off} = |I_{B1} - I_{B2}|$

Typical values:

I_B= 10nA, I_{off}= 10nA (BJT's)
I_{B1} I_{off} ⟶ PA. (FET's)



Add an R_3 at terminal 2

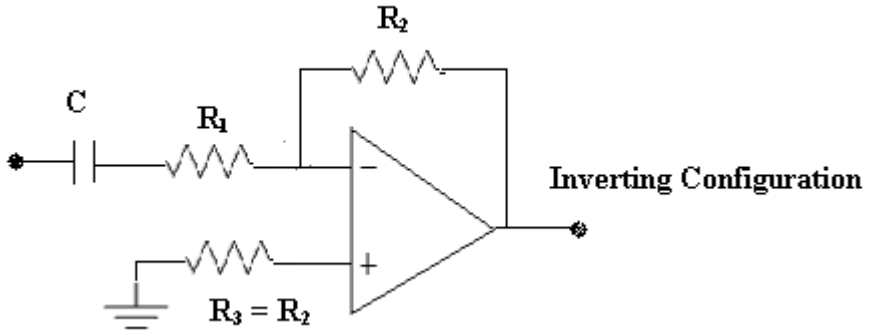


$$V_O = -I_{B2}R_3 - (\frac{I_{B2}R_3}{R_1} - I_{B1})R_2$$

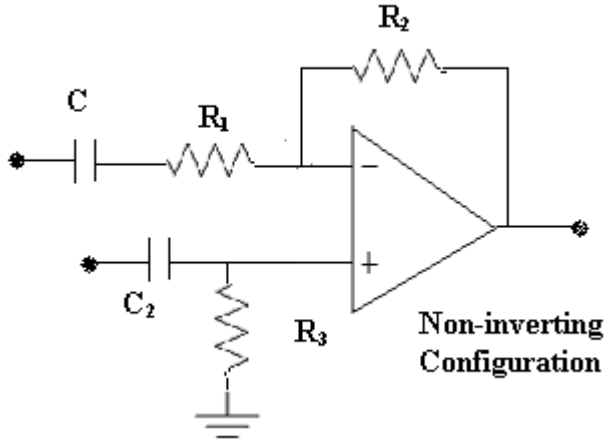
$$if \quad I_{B1} \approx I_{B2} = I_B \qquad \therefore V_O = I_B[R_2 - R_3(1+\frac{R_2}{R_1})]$$

$$V_O \to 0 \quad if \quad R_2 = R_3(1+\frac{R_2}{R_1})$$

$$or \qquad R_3 = \frac{R_1R_2}{R_1+R_2}$$



C is to minimize DC input offset voltage
R_3 is to minimize input bias current effect.



Note: when using ad coupling always provide a dc path to ground.