Slew Rate

\[ \frac{v_O}{v_I} = \frac{1}{1 + \frac{s}{\omega}} \]  \hspace{1cm} (1)

if \[ v_I(t) = V \cdot u(t) \]  \hspace{1cm} (2)

then \[ v_O(t) = V(1 - e^{-t/\tau}) \]  \hspace{1cm} (3)

where \[ \tau = 1/\omega \]
For $V$ large, the op amp output will be unable to rise at the rate predicted by equation 3. When the op amp output is unable to rise at the rate predicted by equation 3, i.e., $V/\tau$ ($\omega=0$), it is said to be slew-rate limited – or slewing.

The slew-rate (SR) is the maximum possible rate of change of the op amp output voltage.

$$SR = \left. \frac{dv_o}{dt} \right|_\text{max} \quad V/\mu\text{sec}$$

Origin of slew rate

At $t=0$, $v_2=v_1=V$, $v_o=0$; i.e., $v_1=0$, $v_{id}=V$.

$\therefore$ the trans conductance will saturate.
\[ I_O = I_{\text{max}} \]

\[ v_o(t) = \frac{1}{C} \int i dt \]

Hence
\[ \frac{1}{C} \int_{0}^{t} I_{\text{max}} \cdot dt = \frac{I_{\text{max}}}{C} \cdot t \quad \text{or} \quad SR = \frac{I_{\text{max}}}{C} \]

**Full-Power Bandwidth**

Op-amp slew-rate limiting can cause nonlinear distortion in sinusoidal waveforms.

\[ v_i = \hat{V}_i \sin \omega t \]

\[ \frac{dv_i}{dt} = \omega \hat{V}_i \cos \omega t \]

\[ \frac{dv_i}{dt} \bigg|_{\text{max}} = \omega \hat{V}_i \]

also \[ \frac{dv_o}{dt} \bigg|_{\text{max}} = \omega \hat{V}_o \]
The frequency at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting is called the full-power bandwidth, \( f_M \).

\[
\omega_M V_{o\text{max}} = SR
\]

\[
\therefore f_M = \frac{SR}{2\pi V_{o\text{max}}}
\]

For \( V_o < V_{o\text{max}} \) (= rated o/p voltage), slew rate distortion will appear at a frequency \( \omega \) given by:

\[
\omega V_o = SR
\]

or \( \omega V_o = \omega_M V_{o\text{max}} \)

i.e., \( V_o = V_{\text{max}} \left( \frac{\omega_M}{\omega} \right) \)

**COMMON-MODE REJECTION**

\[ A_{cm} = \text{common-mode gain} = \frac{v_o}{v_{1\text{cm}}} \]

\[ \text{vid} = v_2 - v_1 \]

\[ v_{1\text{cm}} = \frac{(v_2 + v_1)}{2} \]

\[ v_o = A v_{1\text{d}} + A_{cm} v_{1\text{cm}} \]

Common-mode rejection ratio (CMRR)

\[
CMRR = \left\| \frac{A}{A_{cm}} \right\| \quad \text{or in dB, } = 20 \log_{10} \frac{|A|}{A_{cm}}
\]
INPUT AND OUTPUT RESISTANCES

DC Problems

Offset voltage:
The DC output offset will change the bias conditions and drive the amplifier to saturation. To avoid this problem, we capacitively coupled amplifiers.

\[ V_{\text{off}} = V_0/A_0 \quad \text{offset-free Op Amp} \]

\[ V_{\text{out}} = V_{\text{off}} (1+R_2/R_1) \]

In this arrangement, \( V_{\text{off}} \) will be amplified.
C is selected large enough to appear almost as a short circuit for input frequencies – i.e.,
\[ \frac{1}{\omega C} \approx 0 \quad \omega \in [\omega_{\min}, \omega_{\max}] \]

**Input Bias Currents**

The average value \( I_B \) is called the input bias current. \( I_B = \frac{I_{B1} + I_{B2}}{2} \)

Input offset current: \( I_{\text{off}} = |I_{B1} - I_{B2}| \)

Typical values:
\( I_B = 10 \text{nA}, \quad I_{off} = 10 \text{nA} \quad \text{(BJT's)} \)

\( I_{B1} \quad I_{off} \quad \rightarrow \quad \text{PA. (FET's)} \)

Add an \( R_3 \) at terminal 2
\[ V_o = -I_{b2}R_3 - \left( \frac{I_{b2}R_3}{R_1} - I_{b1} \right)R_2 \]

if \( I_{b1} \approx I_{b2} = I_b \) \[ \therefore V_o = I_b \left[ R_2 - R_3 \left( 1 + \frac{R_2}{R_1} \right) \right] \]

\[ V_o \rightarrow 0 \quad \text{if} \quad R_2 = R_3 \left( 1 + \frac{R_2}{R_1} \right) \]

or \[ R_3 = \frac{R_1 R_2}{R_1 + R_2} \]

C is to minimize DC input offset voltage

R_3 is to minimize input bias current effect.

Note: when using ad coupling always provide a dc path to ground.